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DATE: Tuesday, May 11, 2004

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☐	L24	(fault resilient or fault$1resilient) and bootstrap$	1
☐	L23	(fault resilient or fault$1resilient)	49
☐	L22	(fault resilient or fault$1resilient) near10 bootstrap$	0
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☐	L8	L6 and bootstrap$	2
☐	L7	L6 same bootstrap$	0
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☐	L1	6611911.pn.	1

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L13: Entry 2 of 6 File: USPT Jul 15, 2003

DOCUMENT-IDENTIFIER: US 6594786 B1
TITLE: Fault tolerant high availability meter

Brief Summary Text (6):
The vast majority of servers are supplied with conventional cost-effective availability features, such as backup. Enhanced hardware technologies have been developed to improve availability in excess of 95%, including automatic server restart (ASR), uninterruptable power supplies (UPS), backup systems, hot swap drives, RAID (redundant array of inexpensive disks), duplexing, manageable ECC (error checking and correcting), memory scrubbing, redundant fans, and hot swap fans, fault-resilient processor booting, pre-failure alerts for system components, redundant PCI (peripheral component interconnect) I/O (input/output) cards, and online replacement of PCI cards. The next segment of server usage is occupied by high-availability servers with uptimes in excess of 99.9%. These servers are used for a range of needs including internet services and client/server applications such as database management and transaction processing. At the highest end of the availability spectrum are systems that require continuous availability and which cannot tolerate even momentary interruptions, such as air-traffic control and stock-floor trading systems.

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L17: Entry 4 of 43 File: USPT Feb 3, 2004

DOCUMENT-IDENTIFIER: US 6687818 B1
TITLE: Method and apparatus for initiating execution of an application processor in a clustered multiprocessor system

Brief Summary Text (19):
In an Intel MP compliant system, one of the processors is designated as the bootstrap processor (BSP) at system initialization by the system hardware or by the system hardware in conjunction with the BIOS. The remaining processors are designated as application processors (APs). The BSP is responsible for booting the operating system and initiating execution of the APs.

CLAIMS:

1. A multiprocessor data processing system comprising: two or more processors; one of the processors selected as a bootstrap processor (BSP) for executing an operating system, and selected ones of the remaining processors selected as application processors (AP), each of the application processors having a pre-assigned processing module ID associated therewith; storage means including a processing module ID section and a startup address code section, each of the application processors capable of reading the processing module ID and the startup address from said storage means; each of the application processors including comparing means for comparing their pre-assigned processing module IDs against the processing module ID section stored in said storage means; and the operating system including means for initiating execution of one of the application processing modules at a selected startup address by writing a matching processing module ID into the processing module ID section and a desired startup address into the startup address code section of said storage means, whereby the AP with the matching processing module ID jumps to the startup address.

4. A multiprocessor data processing system comprising: a first cluster including: at least one first processing module, wherein each first processing module has a corresponding interrupt controller associated therewith; a first hierarchical cluster manager device; and a first interrupt controller bus for communicating messages between the interrupt controllers of the at least one first processing modules and the first hierarchical cluster manager device; a second cluster including: at least one second processing module, wherein each second processing module has a corresponding interrupt controller associated therewith; a second hierarchical cluster manager device; a second interrupt controller bus for communicating messages between the interrupt controllers of the at least one second processing modules and the second hierarchical cluster manager device; means for providing messages between the first hierarchical cluster manager and the second hierarchical cluster manager; selected ones of the first and second processing modules are included in a partition; each of the selected first and second processing modules of the partition having a pre-assigned processing module IDs associated therewith; one of the selected first and second processing modules of the partition being a bootstrap processing (BSP) module for executing an operating system, and the remaining ones of the selected first and second processing modules being application processing (AP) modules; storage means for providing a storage space including a processing module ID section, a valid flag section and a startup address code section, each of the application processing modules including

comparing means for comparing their pre-assigned processing module IDs against the processing module ID stored in the processing module ID section of said storage space; and the BSP module including means for initiating execution of one of the application processing modules in the partition at a selected startup address by writing a matching processing module ID into the processing module ID section, a desired startup address into the startup address code section, and a valid flag into the valid flag section of said storage space, whereby the AP with the matching processing module ID reads the storage space, jumps to the startup address, and resets the valid flag section.

13. A multiprocessor data processing system comprising: a bootstrap processing module for executing an operating system; one or more application processing modules, wherein each of the application processing modules includes an ID register for storing a unique module ID; a safe memory area having a processing module ID section and a startup address section, wherein the bootstrap processor includes means for selectively providing a processing module ID and a startup address to the processing module ID section and a startup address section, respectively, of the safe memory area; each of the application processing modules having comparing means for comparing the unique module ID stored in the ID register with the processing module ID stored in the processing module ID section of the safe memory area; each of the application processing modules further having reading means for reading the startup address from the startup address section of the safe memory area at least when the unique module ID stored in the ID register matches the processing module ID stored in the processing module ID section of the safe memory area; and each of the application processing modules having jumping means for initiating processor execution at the startup address read by said reading means.

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L21: Entry 3 of 5 File: USPT Dec 5, 2000

DOCUMENT-IDENTIFIER: US 6158000 A
TITLE: Shared memory initialization method for system having multiple processor capability

Abstract Text (1):
A multiprocessor computer system is provided with a BIOS that allows parallel execution of system initialization tasks by at least two processors to reduce system boot-up time. At power-on, one of the processors is designated as a bootstrap processor and the remaining processors are designates as application processors. The processors are coupled to a shared memory module by a shared processor bus. The bootstrap processor is configured to instruct the application processor to test and initialize memory locations in the shared memory module while the bootstrap processor proceeds with other system initialization tasks which may include determining the system configuration, initializing peripheral devices, testing the keyboard, and setting up the BIOS data area with configuration information. After completing its tasks, the bootstrap processor determines whether the application processor has completed the memory test, and if so, the bootstrap processor proceeds to locate and execute an operating system. It is expected that testing and initializing memory in parallel with other system initialization tasks will advantageously reduce system boot-up time in multiprocessor systems having large memories (e.g. 1-4 gigabytes).

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L13: Entry 3 of 6 File: USPT Dec 17, 2002

DOCUMENT-IDENTIFIER: US 6496790 B1
TITLE: Management of sensors in computer systems

Detailed Description Text (5):
FIG. 2 shows an example of system management baseboard 102, including an application specific integrated circuit (ASIC) 103 to implement the server management functions. (Of course, ASIC 103 is not necessary and the hardware implementing the system management may alternatively consist of several different chips.) ASIC 103 includes a micro-controller silicon core, which includes the functionality of BMC 104 as well as the functionality of a front panel controller (FPC) 105 to control a front panel and user inputs, and possibly a power supply controller. A RISC processor (not shown) controls various server management functions, such as the system power/reset control, sensor monitoring, system initialization, fault resilient booting (FRB), etc. Although not shown in FIG. 2, ASIC 103 also contains a General Purpose Input/Output (GPIO) interface for programmable pins, Universal Adaptive Receiver/Transmitters (UARTs) to connect to other devices.